Power

Full name	Status	Vendor	Geometry	Variation	Feature
LDO	●	HLMC	40nm	LP	1.Input Voltage Range of 2.1V to 2.9V with fixed Output Voltage 1.1V 2.Maximum Loading Current 200mA
	●				1.Input Voltage Range of 2.4V to 3.6V with fixed Output Voltage 1.1V 2.Maximum Loading Current 200mA
	●				1.Input Voltage Range of 2.4V to 3.6V with fixed Output Voltage 1.1V 2.Maximum Loading Current 100mA
	●				1.Input Voltage Range of 2.4V to 3.6V with fixed Output Voltage 1.1V 2.Maximum Loading Current 50mA
Capless LDO	●		55nm		1.The input voltage range of 1.1V~1.3V 2.Maximum dropout voltage 100mV
DC/DC	●	TSMC	250nm	BCD	1.Peak Efficiency: 95% 2.Integrated 55-mΩ/50-mΩ MOSFETs
Ultra-low power LDO (LV/5V转1.2)	●	HHNEC	130nm	EF	1.Ultra-low power LDO static current (<1uA in typical case) 2.10mA low dropout regulator with input switched power supply

● Production ○ Silicon Proven