ADC&DAC

Category	Status	Vendor	Geometry	Variation	Feature
12-bit SAR ADC	●	HLMC	55nm	LP	1. 2MHz Sample Rate 2. 63.1dB SNDR at 12 Bits
10-bit SAR ADC	●				1. Output 10 bit Unsigned Codes 2. 50dB SNDR @Fin=20MHz
12-bit IQ pipeline-ADC	●				1. Differential Input Range Vp-p=1V 2. Typical ENOB>10.8bit
10-bit DAC	●				1. 250MHz system clock frequency 2. 10-bit digital data input
10-bit SAR ADC	●		40nm		1. 1MHz Sample Rate 2. 58.5dB SNDR at 10 Bits
12-bit SAR ADC	●				1. Output 12 bit Unsigned Codes 2. 62dB SNDR @Fin=20MHz
12-bit IQ pipeline-ADC	●				1. Differential Input Range Vp-p=2V 2. Typical SNR: 66dB
10-bit tripple channel DAC	●				1. Up to 250MSPS sample rate 2. 250MHz system clock frequency
8-bit SAR ADC	○	SMIC	65nm	LL	1. Time interleaved architecture for excellent dual channel matching performance. 2.Programmable maximum differential input from 0.5Vdpp to 1.0Vdpp.
12-bit dual channel pipelined ADC	○		55nm		1. Single 1.2V power supply required. 2. I/Q opamp sharing architecture for lower power dissipation and small die size
10-bit dual channel pipeline -ADC	○				1. Single 1.2V power supply required. 2. Time interleaved architecture for excellent dual channel matching performance.
10-bit SAR ADC	○				1. Time interleaved architecture for excellent dual channel matching performance. 2. Fully integrated internal reference generator with no external pins.

Category	Status	Vendor	Geometry	Variation	Feature
12-bit DAC	○	SMIC	55nm	LL	1. Dual 3.3/1.2V power supplies required. 2. Fully integrated internal reference generator with no external pins.
12-bit SAR ADC	●		40nm		1. 2MHz Sample Rate 2. 63dB SNDR at 12 Bits
10-bit video DAC	●				1. Up to 300MHz Sample Rate 2. 10bit Digital Data Input
10-bit video DAC	●				1. Up to 250MHz Sample Rate 2. High SFDR More Than 62dB
12-bit pipeline ADC	○		130nm	RF	1. 3.3V analog supply and 1.2V digital supply operation 2. Unsigned binary digital outputs
Dual Channel 10B25M ADC	○	TSMC	90nm	LP	1. 10bit resolution pipelined analog-to-digital converter. 2. Support both 1-channel @ 50Msps, or 2-channel concurrent sampling @ 25Msps mode, or 6-channel alternative sampling @2Msps.
Dual Channel 10B50M ADC	○		65nm/ 55nm		1. Programmable maximum differential input from 0.5Vdpp to 1.0Vdpp. 2.Input clock frequency of 2MHz to 50MHz.
10-bit DAC	○		65nm		1. Dual +1.2V/+3.3V power supplies required. 2. Very small silicon area of 350um x850um with 1P7M layout structure.
10-bit pipeline-ADC	○		55nm	GP	1. Single 1.0V power supply required. 2. 10bit resolution pipelined analog-to-digital converter
12-bit pipeline-ADC	○		180nm	Generic	1. 1.8V and 3.3V power supplies required. 2. Pixel clock frequency of 27MHz to 108MHz
14-bit DAC	○				1. 3.3V analog and 1.2V digital supply 2. Differential output swing: -1.0V to +1.0V

Category	Status	Vendor	Geometry	Variation	Feature
10-bit Dual Channel DAC	○	HHG	180nm	Generic	1. 1.8V analog and 1.8V digital supply 2. Differential output swing: -0.5V to +0.5V
8-bit pipeline-ADC	○	Cirrus	180nm	Generic	1. High speed pipeline architecture 2. 3.0V analog/digital supply, and 1.8V core digital supply
10-bit dual channel pipeline-ADC	○	Silterra	180nm	Generic	1. 15 ~ 80 MHz data rates 2. Dynamic Power Scaling a. 53dB SNR @ Fin = 10MHz b. 56dBc SFDR @Fin =10MHz
10-bit DAC	○				1. Two Identical Channels 2. 10 to 60MHz update rate 3. 5mA ~ 20mA adjustable full scale output current
10-bit pipeline-ADC	○	UMC	180nm	Generic	1. 1.8V analog supply and 1.8V digital supply operation 2. Differential input range: -0.5V to +0.5V
8-bit pipeline-ADC	○	Toshiba	250nm	Generic	1. 1bit coarse and 7bit fine conversion architecture with folding and interpolation 2. 2.5V (+/-10%) analog supply and 1.5V (+/-10%) digital supply

● Production ○ Silicon Proven